CLAIMS

What is claimed is:

1. An integrated circuit package, comprising:

a substrate having a first surface for mounting a semiconductor die and a second surface defining a via; and

a lead formed with a conductive material to project outwardly from the second surface, where the conductive material is extended from the lead and through the via for coupling to the semiconductor die.

2. The integrated circuit package of claim 1, wherein the via is formed through the substrate to the first surface.

3. The integrated circuit package of claim 2, wherein the conductive material extends along the first surface to form a pad for electrically coupling to the semiconductor die.

4. The integrated circuit package of claim 1, wherein the conductive material is disposed along the second surface from the via to the lead.

5. The integrated circuit package of claim 1, wherein the conductive material includes copper.

6. The integrated circuit package of claim 5, wherein the conductive material includes plated copper.

7. The integrated circuit package of claim 1, wherein the lead projects from the second surface a distance of at least fifty micrometers.

8. The integrated circuit package of claim 1, wherein the substrate is formed with a dielectric material.

9. The integrated circuit of claim 8, wherein the dielectric material includes bismaleimide-triazine resin.

10. An integrated circuit, comprising:

a semiconductor die;

a substrate having first surface for mounting the semiconductor die and a second surface defining a via;

a signal path formed with a first material that is disposed along the first surface and through the via to route a signal between the second surface and the semiconductor die; and

a lead formed with the first material for coupling to the signal path, where the lead projects a distance from the second surface for receiving the signal.

11. The integrated circuit of claim 10, wherein the substrate is formed with a second material.

12. The integrated circuit of claim 11, wherein the first material comprises a conductive material and the second material comprises an insulator.

13. The integrated circuit of claim 10, wherein the signal path extends along the first surface to form a pad, further comprising a bonding wire for coupling the signal from the pad to the semiconductor die.

14. The integrated circuit of claim 10, wherein the signal path is routed along the second surface to form an access pad for disposing the lead.

15. The integrated circuit of claim 14, wherein the access pad is formed with a first thickness of the conductive material and the lead is formed with a second thickness of the conductive material.

16. The integrated circuit of claim 14, wherein the signal path is extended along the second surface and the lead is projected from a surface of the access pad.

17. A method of operating an integrated circuit, comprising the steps of:

providing a substrate having a first surface for mounting a semiconductor die and defining a via;

applying a signal to a conductive material that is disposed to project from a second surface of the substrate; and

routing the signal along the conductive material and through the via to the first surface for coupling to the semiconductor die.

18. The method of claim 17, wherein the step of routing includes the step of routing the signal through plated copper toward the second surface.

19. A method of making an integrated circuit, comprising the step of plating a conductive material to project outwardly from a first surface of a substrate to form a first lead of the integrated circuit.

20. The method of claim 19, further comprising the step of mounting a semiconductor die to a second surface of the substrate.

21. The method of claim 20, further comprising the step of forming a signal path on the second surface with the conductive material.

22. The method of claim 21, further comprising the step of disposing the conductive material in a via defined by the substrate to extend the signal path from the second surface to the first surface of the substrate.

23. The method of claim 22, further comprising the step of disposing the conductive material on the first surface to extend the signal path from the via to the first lead.

24. The method of claim 23, wherein the step of disposing the conductive material on the first surface includes the step of forming an access pad on the first surface.

25. The method of claim 23, further comprising the steps of:
disposing a photoresist layer on the first surface;
patterning the photoresist layer to expose the access pads; and
plating the conductive material on the access pads.

26. The method of claim 25, wherein the step of patterning includes the step of forming an opening in the photoresist layer over the access pads.

27. The method of claim 26, wherein the step of plating includes the step of plating the conductive material within the opening.

28. The method of claim 21, further comprising the step of wire bonding the signal path to a node of the semiconductor die to couple a signal between the node and the first lead.

29. The method of step 19, further comprising the step of forming a solder mask on the first surface between the first lead and a second lead of the integrated circuit.

30. The method of claim 29, wherein the step of forming includes the step of forming the solder mask after the step of plating.

31. The method of claim 19, wherein the step of plating includes the step of plating the conductive material in an outward direction for routing a current through the first lead that flows parallel to the outward direction.

32. A method of forming an integrated circuit, comprising the steps of:

providing a substrate having a first surface for mounting a semiconductor die; and

plating a conductive material to extend outwardly from a second surface of the substrate to form a lead of the integrated circuit.

33. The method of claim 32, wherein the step of plating includes the step of disposing the conductive material to a height for attaching the lead to a mounting surface.

34. The method of claim 33, wherein the step of disposing includes the step of disposing the conductive material to the height of at least fifty micrometers.

35. The method of claim 33, wherein the step of disposing includes the step of forming the lead to a height that maintains a spacing between the substrate and the motherboard.

36. A method of making an integrated circuit, comprising the steps of:

mounting a semiconductor die to a first surface of a substrate;

disposing a conductive material along the first surface and through a via of the substrate to form a signal path of the integrated circuit between the first and a second surface of the substrate; and

disposing the conductive material on the second surface to form a lead of the integrated circuit that is electrically coupled to the signal path.

37. The method of claim 36, wherein the step of disposing includes the step of plating the conductive material to project outwardly from the second surface.